19-2042; Rev 0; 5/01

MAXIM

2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

General Description

The MAX4686/MAX4687/MAX4688 low on-resistance (R_{ON}), low-voltage analog switches operate from a single +1.8V to +5.5V supply. The MAX4686/MAX4687 are single-pole/single-throw (SPST) analog switches, and the MAX4688 is a single-pole/double-throw (SPDT) analog switch. The MAX4686 is a normally open (NO) switch, and the MAX4687 is a normally closed (NC) switch. The MAX4688 has one normally open (NO) switch and one normally closed (NC) switch.

When powered from a 3V supply these devices feature 2.5Ω (max) R_{ON}, with 0.4Ω (max) R_{ON} matching and 1Ω (max) flatness. The MAX4686/MAX4687/MAX4688 offer fast switching speeds (t_{ON} = 30ns max, t_{OFF} = 12ns max). The MAX4688 offers break-before-make action.

The digital logic inputs are 1.8V logic compatible from a +2.7V to +3.3V supply. The MAX4686/MAX4687/MAX4688 are available in the chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 1.50mm x 1.02mm area. The 3 x 2 array of solder bumps are spaced with a 0.5mm bump pitch.

Applications

MP3 Players
Cellular Phones
Power Routing
Battery-Operated Equipment
Relay Replacement
Audio and Video Signal Routing
Communications Circuits
PCMCIA Cards
Cellular Phones
Hard Drives

Features

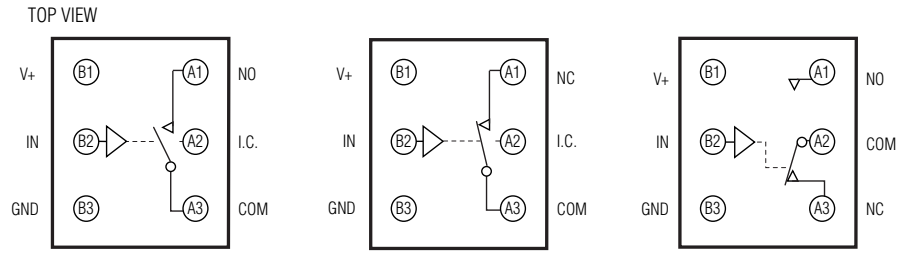
- **6-Bump, 0.5mm Pitch, UCSP (Package Pending Full Qualification Expected Completion Date 6/30/01. See *UCSP Reliability* Section for More Details.)**
- **R_{ON}**
  2.5Ω max (+3V Supply)
  10Ω max (+1.8V Supply)
- **0.4Ω max R_{ON} Match Between Channels**
- **1Ω max R_{ON} Flatness Over Signal Range**
- **Low Leakage Currents Over Temperature**
  0.5nA (max) at T_A = +25°C
- **Fast Switching: t_{ON} = 30ns, t_{OFF} = 12ns**
- **Guaranteed Break-Before-Make (MAX4688)**
- **+1.8V to +5.5V Single-Supply Operation**
- **Rail-to-Rail® Signal Handling**
- **Low Crosstalk: -95dB (100kHz)**
- **High Off-Isolation: -90dB (100kHz)**
- **1.8V Logic Compatible**

Ordering Information

PART	TEMP. RANGE	BUMP-PACKAGE	TOP MARK
MAX4686EBT	-40°C to +85°C	6 UCSP*	AAI
MAX4687EBT	-40°C to +85°C	6 UCSP*	AAJ
MAX4688EBT	-40°C to +85°C	6 UCSP*	AAK

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Pin Configurations/Functional Diagrams/Truth Table



SWITCHES SHOWN FOR LOGIC "0"

MAX4686/MAX4687/MAX4688		
IN	**NO**	**NC**
0	OFF	ON
1	ON	OFF

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
UCSP is a trademark of Maxim Integrated Products, Inc.

2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND
V+, IN .....-0.3V to +6V
COM, NO, NC (Note1).....-0.3V to (V+ + 0.3V)
Continuous Current NO, NC, COM .....±100mA
Peak Current NO, NC, COM
(pulsed at 1ms, 10% duty cycle) .....±200mA

Continuous Power Dissipation (T_A = +70°C)
3 x 2 UCSP (derate 10.1mW/°C at +70°C) 808mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Bump Reflow Temperature .....+235°C

Note 1: Signals on NO, NC, and COM exceeding V+ are clamped by an internal diode. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at 3V and T_A = +25°C.) (Notes 2, 8)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}		T_{MIN} to T_{MAX}	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, V_{NC} = 0 to V+, I_{COM} = 10mA	+25°C		1.5	2.5	Ω
			T_{MIN} to T_{MAX}			3.5	
On-Resistance Match Between Channels (MAX4688 only) (Note 4)	ΔR_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, I_{COM} = 10mA	+25°C		0.3	0.4	Ω
			T_{MIN} to T_{MAX}			0.5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 2.7V, V_{NO} or V_{NC} = 0 to V+, I_{COM} = 10mA	+25°C		0.5	1	Ω
			T_{MIN} to T_{MAX}			1	
NO, NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = 3.3V; V_{COM} = 0.3V or 3V; V_{NO} or V_{NC} = 3V, 0.3V	+25°C	-0.5	±0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM Off-Leakage Current (Note 3)	$I_{COM\_(OFF)}$	V+ = 3.3V; V_{COM} = 0.3V or 3V; V_{NO} or V_{NC} = 3V, 0.3V	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM On-Leakage Current (Note 3)	$I_{COM\_(ON)}$	V+ = 3.3V; V_{COM} = 3V or 0.3V; V_{NO} or V_{NC} = 3V, 0.3V, or floating	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 3)	t_{ON}	V_{NO} or V_{NC} = 1.5V, Figure 2	+25°C		20	30	ns
			T_{MIN} to T_{MAX}			35	
Turn-Off Time (Note 3)	t_{OFF}	V_{NO} or V_{NC} = 1.5V, Figure 2	+25°C		10	12	ns
			T_{MIN} to T_{MAX}			15	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at 3V and T_A = +25°C.) (Notes 2, 8)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Break-Before-Make (MAX4688 only) (Note 3)	t_{BBM}	V_{NO}, V_{NC} = 1.5V, Figure 3	+25°C		8		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 4	+25°C		40		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out, Figure 5	+25°C		200		MHz
Off-Isolation (Note 6)	V_{ISO}	C_L = 5pF, R_L = 50Ω, f = 100kHz, Figure 5	+25°C		-90		dB
Crosstalk (MAX4688 only) (Note 7)	V_{CR}	C_L = 5pF, R_L = 50Ω, f = 100kHz, Figure 5	+25°C		-95		dB
Total Harmonic Distortion	THD	R_L = 600Ω, 2Vp-p, f = 20Hz to 20kHz	+25°C		0.06		%
NO, NC Off-Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, Figure 6	+25°C		12		pF
COM Off-Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6	+25°C		12		pF
Switch On-Capacitance	$C_{(ON)}$	f = 1MHz, Figure 6	+25°C		35		pF
DIGITAL I/O							
Input Logic High	V_{IH}		T_{MIN} to T_{MAX}	1.4			V
Input Logic Low	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Logic Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0 or V+	T_{MIN} to T_{MAX}	-1		1	µA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Supply Current	I+	V+ = 3.3V, V_{IN} = 0 or V+	T_{MIN} to T_{MAX}	-1		1	µA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$, between switches.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 6: Off Isolation = $20\log_{10} (V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

Note 7: Between switches.

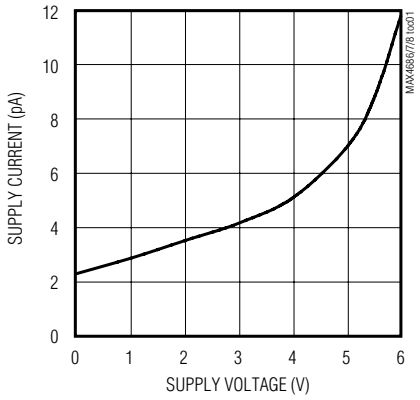
Note 8: UCSP parts are 100% tested at +25°C only and guaranteed by correlation at the full hot-rated temperature.

2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

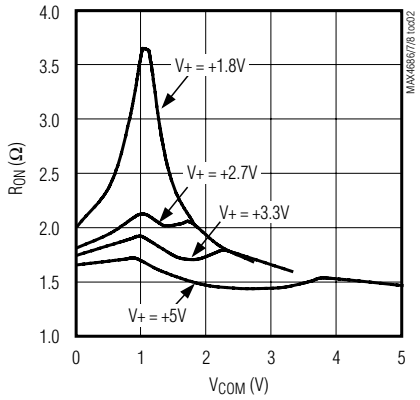
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

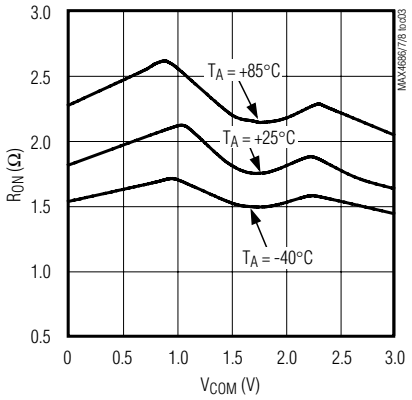
SUPPLY CURRENT vs. SUPPLY VOLTAGE



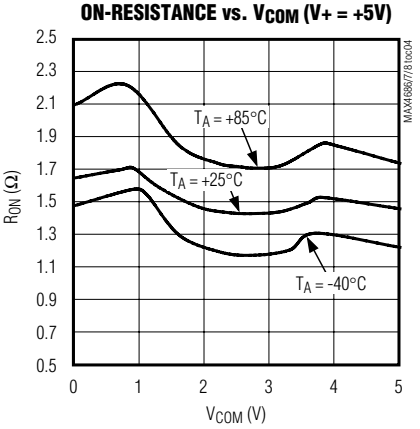
ON-RESISTANCE vs. V_{COM}



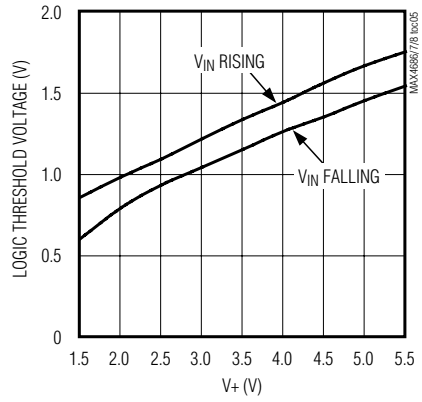
ON-RESISTANCE vs. V_{COM} (V+ = +3V)



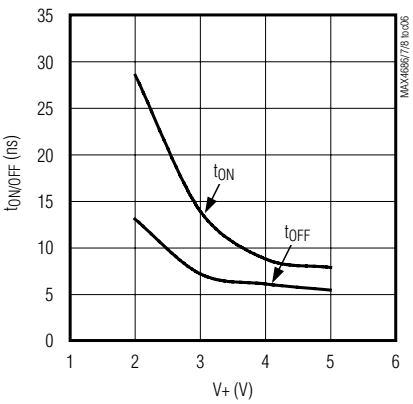
ON-RESISTANCE vs. V_{COM} (V+ = +5V)



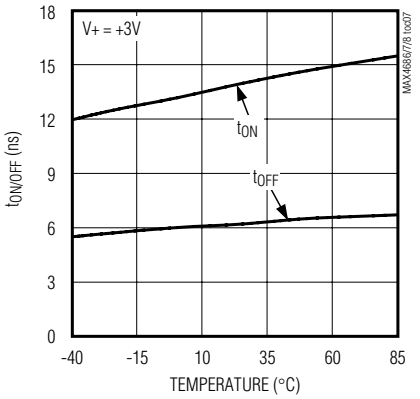
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



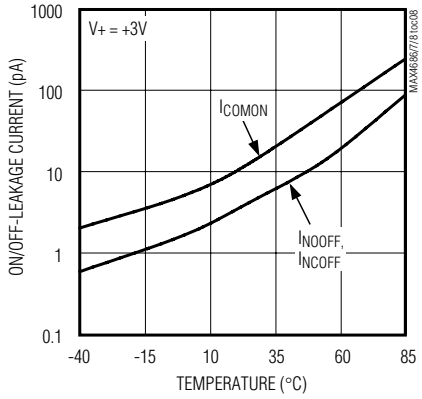
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



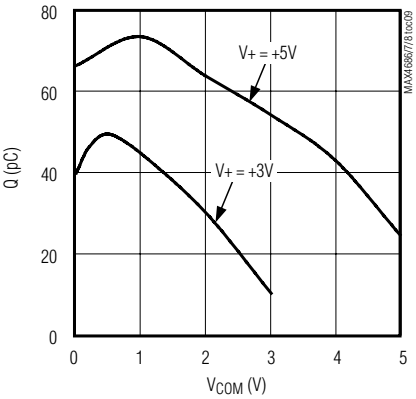
TURN-ON/OFF TIME vs. TEMPERATURE



ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



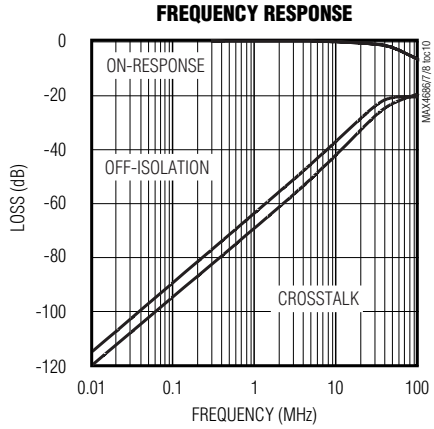
CHARGE INJECTION vs. V_{COM}

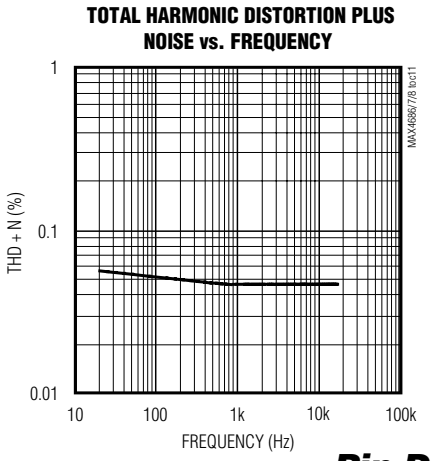


2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

BUMP			NAME	FUNCTION
MAX4686	MAX4687	MAX4688		
B1	B1	B1	V+	Positive Supply Voltage Input
B2	B2	B2	IN	Digital Control Input
B3	B3	B3	GND	Ground
—	A1	A3	NC	Analog Switch, Normally Closed Terminal
A3	A3	A2	COM	Analog Switch, Common Terminal
A1	—	A1	NO	Analog Switch, Normally Open Terminal
A2	A2	—	I.C.	Internally Connected

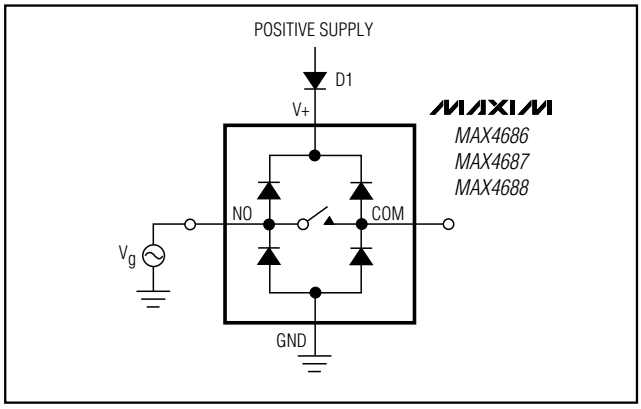


Figure 1. Overvoltage Protection Using External Blocking Diodes

Applications Information

Logic Inputs

Where the MAX4686/MAX4687/MAX4688 have a +3.3V supply, IN may be driven low to GND and driven high to 5.5V. Driving IN rail-to-rail minimizes power consumption. Logic inputs accept up to +5.5V regardless of supply voltage.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in R_{ON} (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO, NC, and COM pins are both inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

CAUTION: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.

2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small-signal diode (D1) as shown in Figure 1. Adding a protection diode reduces the analog range to a diode drop (about 0.7V) below V+ (for D1). R_{ON} increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V.Protection diode D1 also protects against some overvoltage situations. No damage will result on Figure 1's circuit if the supply voltage is below the absolute maximum rating and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin.

UCSP Package Consideration

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale Package).

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a CSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

Test Circuits/Timing Diagrams

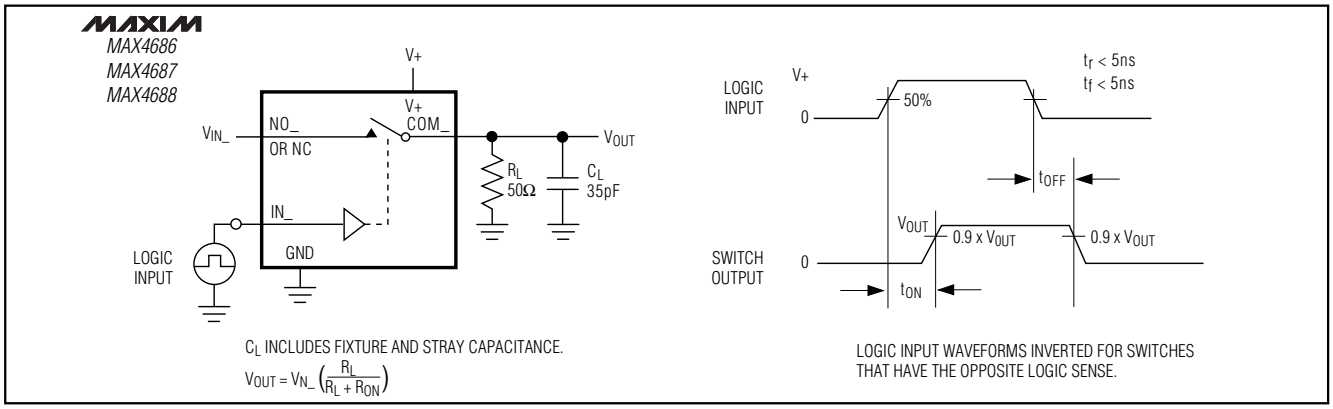


Figure 2. Switching Time

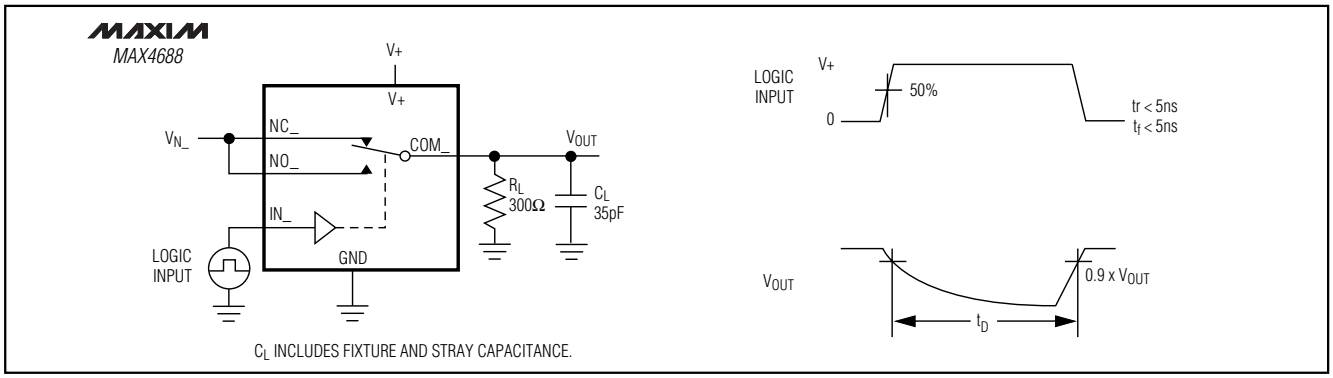


Figure 3. Break-Before-Make Interval (MAX4688 only)

Test Circuits/Timing Diagrams (continued)

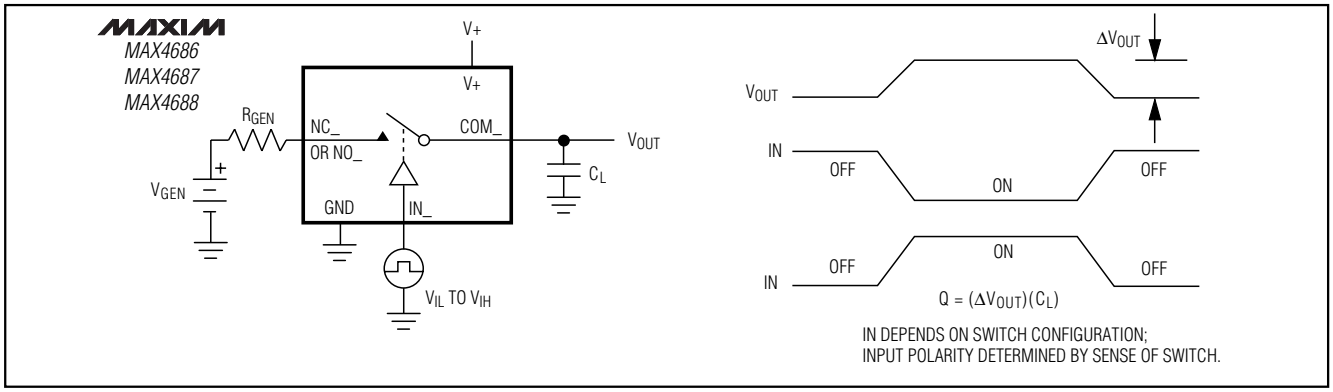


Figure 4. Charge Injection

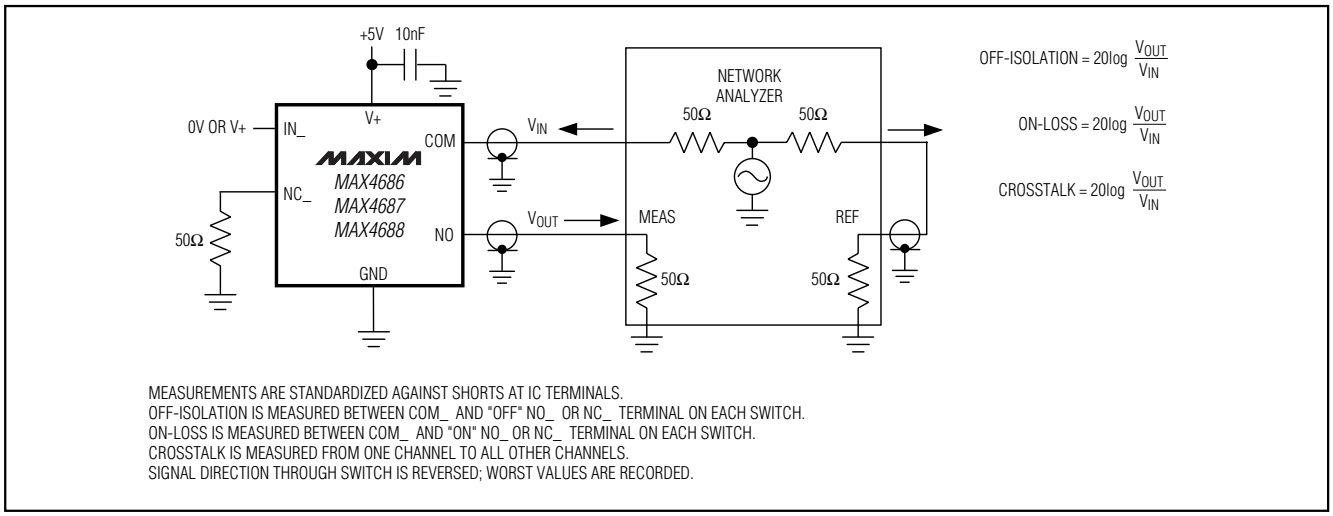


Figure 5. Off-Isolation/On-Channel Bandwidth, Crosstalk

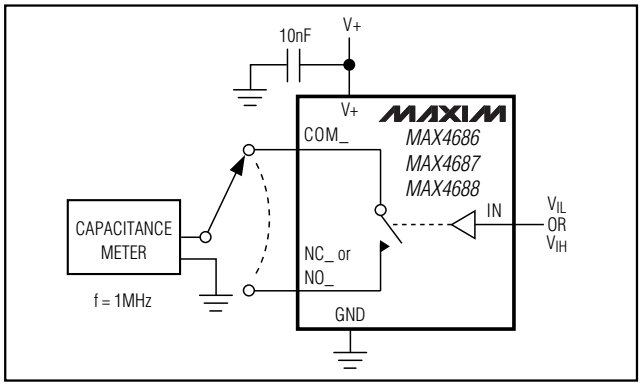


Figure 6. Channel Off/On-Capacitance

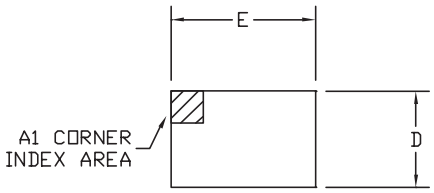
Chip Information

TRANSISTOR COUNT: 150

2.5Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

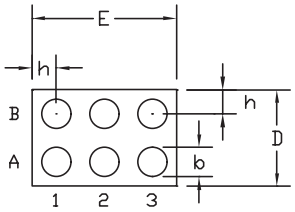
Package Information

6L,UCSP.EPS

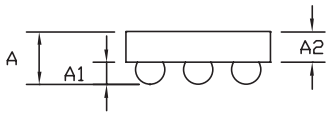


TOP VIEW

SYMBOL	DIMENSIONS
A	0.022 ±.002
D	0.040 ±.002
E	0.059 ±.002
e	0.0197 BASIC
b	ø 0.0120 BASIC
A1	0.009±.0015
A2	0.013 Ref.
h	0.010 Ref.



BOTTOM VIEW



SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. MEETS JEDEC MO195.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 6L UCSP, 3x2

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0097	A	1/1